IEEE ICMTS 2011

Radiation effects upon the mismatch of identically laid out transistor pairs

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ABSTRACT

This paper presents the DC behavior of transistors with finger layout and with gate enclosed layout in a 0.18µm CMOS technology under the influence of gamma-radiation. The threshold voltage shift and the drain current mismatch before and after irradiation has been investigated up to a total ionizing dose of 100kGy.

INTRODUCTION

The employment of electronics in nuclear environments has gotten a fair chair of attention due to several research projects and applications. Standard CMOS technologies look like a good candidate for radiation hard design, especially when gate oxides keep on getting smaller [1]. This is shown in the harsh radiation environment at the Large Hadron Collider (LHC) which requires radiation hard ASICs. The International Thermonuclear Experimental Reactor (ITER) is also an application of interest which will be built in Cadarache, France. Another example is the MYRRHA (Multi-purpose Hybrid Research Reactor for High-tech Applications) reactor which is under development at the SCK-CEN, the Belgian Nuclear Research Institute in Belgium. This is an accelerator driven sub-critical reactor using liquid metal (Pb-Bi) for cooling and also acts as spallation target for the proton accelerator. One of the many challenges for these reactors is the development of specialized electronics. Therefore dedicated ASICs [2] will need to be designed because commercial off the shelf components cannot withstand the high radiation doses (> 100kGy) that will build up near the reactor core or harsh nuclear environment.

The importance of the standard deviation in device parameters (device mismatch) of CMOS technologies has been shown of great importance in analog circuit design [3]. It has been shown that identically laid out transistor pairs show a mismatch in drain current. This can be described by the following formula [4].

$$\frac{\Delta(I_d)}{I_d} = \left.\frac{\Delta I_D}{I_D}\right|_{\Delta V_{TH}} + \left.\frac{\Delta I_D}{I_D}\right|_{\Delta(1/\beta)} \qquad (1)$$

In equation (1) V_{TH} represents the threshold voltage. β is equal to the current-factor ($\mu * C_{ox} * W/L$), here µ is equal to the mobility C_{ox} to the oxide capacitance. W and L are respectively the width and length of the transistor. An in-depth explanation of this formula can be found in [4]. Equation (1) shows that there are two main causes of transistors mismatch, namely threshold voltage mismatch (ΔV_{TH}) and current factor mismatch ($\Delta 1/\beta$). The threshold voltage is known to drift when transistors are exposed to ionising radiation [5], [6]. In [6] it is stated that there is a standard deviation on the threshold voltage shift due to irradiation. **F**or transistors with equal width and length, this standard deviation can be as large as 20% in an 180nm CMOS technology [6]. Furthermore, transistors with different width experience a different sensitivity to TID (total ionising dose) [5]. The different sensitivity to TID of transistors with different gate width is known as the "Radiation-Induced Narrow Channel Effect"(RINCE).

Far less is known about the effect of an increasing radiation dose on the variance of the transistors' parameters which influences the transistor mismatch. The influence of radiation effects on the mismatch of transistor pairs is not well known and will therefore be investigated in this paper.

TEST DEVICES

Different MOS transistors have been tested to investigate the influence of gamma-radiation on the device mismatch parameters. The MOSFETS studied in this work belong to a 0.18µm technology and have an oxide thickness of 4.2 nm. A matching structure was developed to verify the mismatch parameters similar to [4]. It consists of an array of 12 by 6 NMOS transistors. The first 6 rows feature transistors with a classic single finger layout. The next 6 rows consist of enclosed layout transistors (ELT). Enclosed layout transistors are transistors which have a gate that completely surrounds the drain or source of a transistor as shown in Fig.1. In this way all possible current paths between source and drain are controlled by the gate and no parasitic leakage current may flow hence improving the radiation tolerance of the transistor [7]. The ELT devices were laid out and modeled using the guidelines presented in [7].

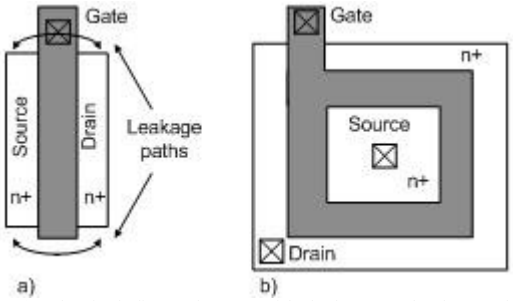

Fig.1 a) Classical finger layout with leakage paths b) Enclosed layout transistor(ELT) with eliminated leakage paths

In the matching structure, the device pairs are placed at equal distances and dummy transistors are added around the edge-transistors which minimizes gradient mismatch. The transistor dimensions are shown in Table 1. The choice of the device dimensions was constrained by the minimum width needed to surround the gate of the smallest enclosed layout transistor**.** 3 transistors (T2, T3 and T4) are chosen with the same ratio as transistor T1 but with different width and length. 4 transistors (T2, T4, T5 and T6) have an equal area but different width en length. In this experiment we were only limited to test one matching structure due to the physical constraints of the irradiation procedure.

TABLE I
TRANSISTOR DIMENSIONS

Regular transistors			**ELT transistors**		
	W (µm)	**L(µm)**		**W(µm)**	**L(µm)**
T1	3.5	0.5	**T7**	3.5	0.5
T2	7.0	1	**T8**	7.0	1
T3	14	2	**T9**	14	2
T4	35	5	**T10**	35	5
T5	28	0.25	**T11**	28	0.25
T6	14	0.5	**T12**	14	0.5

The configuration of the transistor array is shown in Fig. 2.

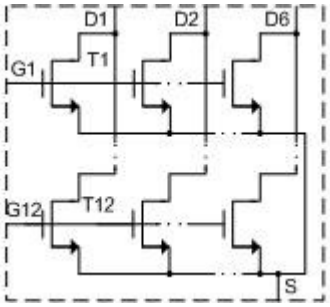

Fig.2 Configuration of the transistors in the matching array.

The transistors in the same column have shared drains. Transistors in the same row have a common gate. They all have shared sources and bulks.

TEST SETUP

Two Keithley 2400 source meters were used to measure the I_{DS}-V_{GS} curve with constant V_{DS}=1.8V. 30 points were measured during the V_{GS} sweep. The threshold voltage was extracted from all transistors using the maximum slope method described in [4]. The threshold voltage was extracted 20 times within 50 minutes on the same transistor to verify the repeatability of the measurement. The standard deviation of the extracted threshold voltage prior to irradiation was 50µV which guarantees the repeatability of the measurements.

The transistors were biased with all ports grounded during irradiation**.** In the case of NMOS transistors the effect of oxide charge trapping will be more significant then interface traps leading to a negative VTH-shift [6]. The IC was irradiated with a dose rate of 1kGy/h up to a total dose of 100kGy. No high temperature annealing was performed. Before and after irradiation the I_{DS}-V_{GS} curve was measured with constant V_{DS} and the threshold voltage and current factor were extracted using the maximum slope method [4].

MEASUREMENT RESULTS

The I_{DS}-V_{GS} curves of all the transistor pairs were measured before and after radiation. First the threshold voltage shift was investigated for both the enclosed layout and the regular NMOS transistors after irradiation. Next, radiation-effects upon the mismatch of identically laid out transistor pairs will be investigated.

A. Radiation induced threshold voltage shift

The radiation induced threshold voltage shift of NMOS transistors as a function of transistor width for this work can be seen in Fig. 3.

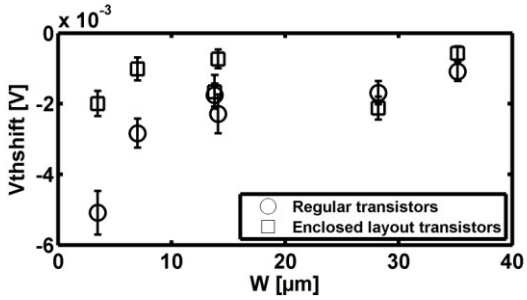

Fig.3 Threshold voltage shift of the transistors after irradiation up to 100kGy for NMOS transistors of different ratios as a function of the transistor width (W). The error bars represent the standard deviation of the voltage shift.

The threshold voltage shifts are averaged over six samples of the same transistor. The error bars represent the standard deviation. These results show that the enclosed layout transistors (ELTs) only show a marginally small threshold voltage shift of maximum -2 mV and no effect of the transistor width, confirming their radiation hardness. For the regular transistors a

maximal shift of -5 mV is obtained. This can be explained by a larger contribution of charge build up in the oxide then the formation of interface states [4]. Also measurements show that the radiation induced threshold voltage shift decreases with increasing width. This result shows the different sensitivity of V_{TH} to TID (total ionizing dose) for transistors with different gate width also referred to as the RINC-effect [8] for a 0.18 µm technology. The value of the standard deviation, represented by the error bars, could influence the mismatch of transistor pairs when the threshold voltage shift is large. This will have to be taken in to account to guarantee the functionality of circuits where drain current mismatch is critical.

B. Mismatch of the transistor pairs

Next the influence of the threshold voltage shift (for a total ionizing dose of 100kGy) on the drain current mismatch of the transistor pairs is investigated. To this end the drain currents of all transistors were measured. The results of the drain current mismatch of the regular and ELT transistors are depicted in Fig. 4 and 5. A small shift of the drain current mismatch can be noticed for small V_{GS} voltages ($\leq \pm$ 0, 65 V). The difference in drain current mismatch becomes smaller with increasing overdrive voltage gradually moving the transistors operating region from weak to strong inversion mode. Fig.4 shows that the drain current mismatch decreases when the area of the transistors rises, which confirms the decrease in drain current mismatch with rising transistor area [4].

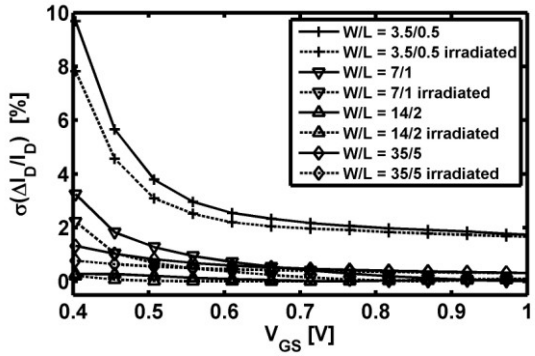

Fig.4 Drain current mismatch before and after gamma irradiation up to 100 kGy the regular transistors

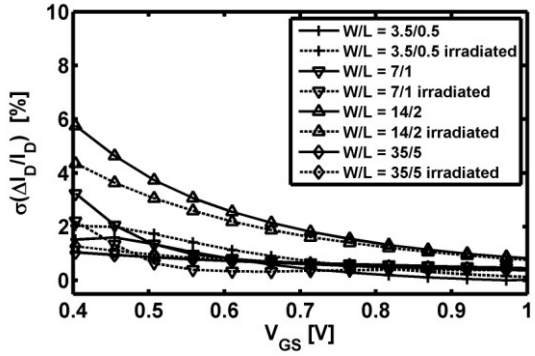

Fig.5 Drain current mismatch before and after gamma irradiation up to 100 kGy the Enclosed Layout transistors.

The same effects can be seen for the ELT transistors in Fig.5. These results illustrate that an irradiation with gamma-rays up to 100kGy only has a small influence the on the drain current mismatch of the transistor pairs. Mismatch is again largest for the small size transistors as can be seen in Figure 5.

Next the threshold voltage mismatch is investigated. Fig.6 and 7 show the extracted values of the threshold voltage mismatch.

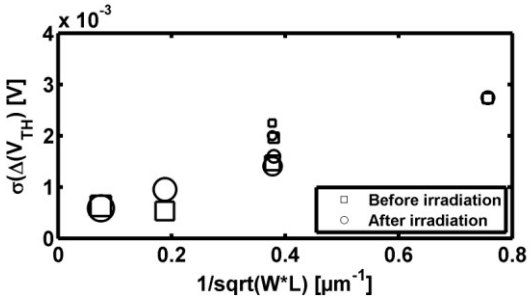

Fig.6 Threshold voltage mismatch between identically designed pairs of the regular transistors before and after gamma-irradiation up to 100 kGy

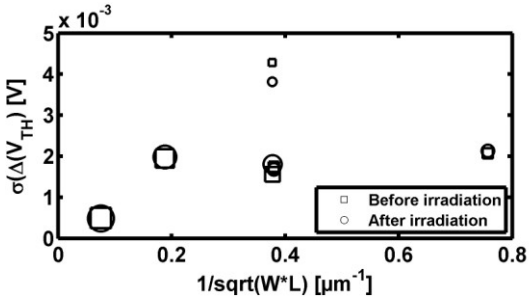

Fig.7 Threshold voltage mismatch between identically designed pairs of the enclosed layout transistors before and after gamma-irradiation up to 100kGy

The squares in the graphs represent the results before irradiation. The circles in the graphs show the standard deviation of the threshold voltage of two identically designed pairs after irradiation with gamma-rays up to 100 kGy. The size of the circles and squares is larger for larger gate lengths.

Fig.6 shows that the mismatch of the threshold voltage becomes smaller for larger transistor areas. Furthermore, from these figures it can be concluded that the threshold voltage shift shown in Fig. 3 only has a minor influence on the threshold voltage mismatch. The transistors threshold voltage mismatch is not influenced by the radiation induced threshold voltage shift. Although these results look promising, for an exact analysis some considerations should be taken. For example an extended analysis could be done at different and higher (>100kGy) radiation doses. In this way the effects of interface traps and charge trapping [5, 6] on the V_{TH} mismatch could be investigated separately. Fig. 7 and 8 shows the standard deviation of the current factor mismatch $\sigma(\beta *(1/\Delta\beta))$. These results also show a minor deflection after irradiation. Hereby, confirming the small

influence of the radiation effects on the drain current mismatch of the transistor pairs.

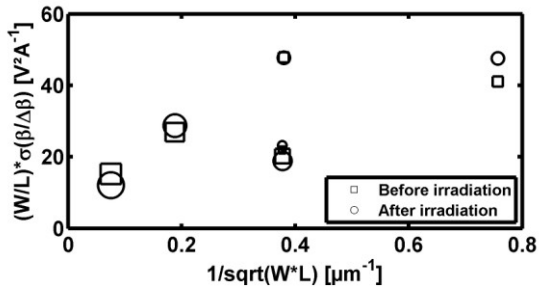

Fig. 8 Standard deviation of the current factor mismatch ($\Delta\beta/\beta$) between identically designed pairs of the regular transistors before and after gamma-radiation up to 100kGy

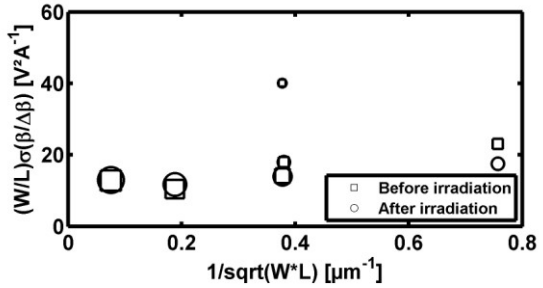

Fig. 9 Standard deviation of the current factor mismatch ($\Delta\beta/\beta$) between identically designed pairs of the enclosed layout transistors before and after gamma-radiation up to 100kGy.

To verify the extracted mismatch parameters, some $\Delta I_D/ I_D$ curves were verified based on the simple mismatch model presented in [4]. The mismatch model described in [4]: is based on equation (2).

$$\frac{\Delta(I_d)}{I_d} = -\frac{g_m}{I_D}\Delta V_{TH} - \beta\Delta\frac{1}{\beta} \qquad (2)$$

In Fig. 10, the full line shows the measured ($\Delta I_D/I_{D)}$ for two transistors. The line with the symbols represents the model which is created through the extracted mismatch data and equation (2). It can be seen that the model fits with the measured data well at high V_{GS}. Except at low V_{GS}-values and for the smallest transistor size the model becomes inaccurate as observed in [4] and Fig. 10.

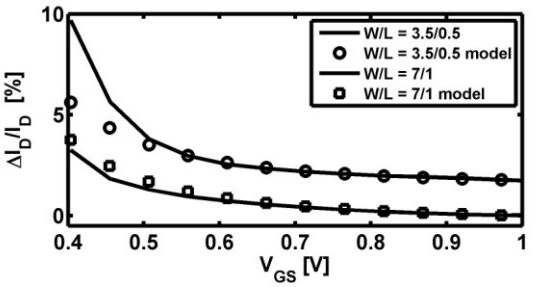

Fig. 10 Experimental data of $\sigma(\Delta I_D/I_D)$-V_{GS}-curves (full lines) together with the model based on equation (2) (symbols).

CONCLUSION

A DC and mismatch characterization of different transistors in a 0.18 µm CMOS technology before and after irradiation up to 100kGy is done. Only a minor shift of the threshold voltage shift was noticeable for both the gate enclosed layout and regular NMOS transistors. For the regular NMOS transistors a significant influence of the transistor width on the threshold voltage shift was observed. The radiation induced threshold voltage shift shows a marginal effect on the transistors drain current and threshold voltage mismatch. The results of this experiment illustrate that the technology is radiation tolerant up to 100kGy and that the mismatch parameters only undergo minor changes. The extracted mismatch parameters were implemented in a model to verify the extracted data. The model matched well to the measured data and showed an accurate fit.

ACKNOWLEDGMENT

The research funded by a Ph.D. grant of the agency for innovation by science and technology (IWT). The authors would like to thank the technical staff of the instrumentation Department at SCK-CEN for their assistance.

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